REMARKS

Claims 1, 3-11, 13-20 and 22-28 are pending in the instant application. Claims 1, 11 and 20 are amended. Claims 2, 12 and 21 are cancelled. Claims 1, 3-11, 13-20 and 22-28 are rejected. No new matter has been added.

112 Rejection

Claims 11-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Amendments made to the Claims herein obviate the 35 U.S.C. 112 rejection of Claims 11-19. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

102 Rejection

Claims 1, 9-11, 16 and 20 are rejected under 35 U.S.C. § 102(e) as being anticipated by Dye (U.S. Patent No. 6,173,381). The Applicant has reviewed the cited references and respectfully submits that the embodiments of the invention as are set forth in Claims 1, 9-11, 16 and 20 are neither anticipated nor rendered obvious by Dye in view of Davis et al.

The Examiner is respectfully directed to independent Claim 1 which is drawn to a controller chip. Claim 1 is presented below in its entirety for the Examiner's convenient reference.

> 1. A controller chip comprising:
>
> a graphics engine operative to manage a memory, the graphics engine comprising an integral interface; and
>
> a first in first out (FIFO) buffer coupled to the graphics engine, the FIFO buffer being accessible by a central processing unit (CPU) through the graphics engine, wherein the graphics engine receives commands from the CPU via the

integral interface, and manages the FIFO buffer via the integral interface wherein data transmittable to the FIFO buffer is transmitted via the integral interface.

Independent Claims 11 and 20 contain limitations similar to those contained in Claim 1. Claims 9-10 depend from Claim 1 and Claim 16 depends from Claim 11 and set forth additional limitations of the claimed invention.

Dye does not anticipate or render obvious the embodiments of the present invention as set forth in Claims 1, 11 and 20. Dye is deficient as Dye does not teach or suggest each of the limitations of Claims 1, 11 and 20 as is required to anticipate or render obvious these Claims. In particular, Dye does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer where "data transmittable to the FIFO buffer is transmitted via the integral interface" as is recited in Claim 1 (independent Claims 11 and 20 contain similar limitations).

It should be appreciated that in order to anticipate or render obvious the embodiment of the invention that is set forth in Claim 1 (Claims 11 and 20 recite limitations similar to those recited in Claim 1) the cited references must teach or suggest, either expressly or inherently, in addition to all of the other limitations of Claim 1, a FIFO buffer and a graphics engine where: (1) the graphics engine includes an integral interface and where (2) data transmittable to the FIFO buffer is transmitted via the integral interface. Applicant respectfully submits that such a system structure and operation is not taught or suggested by Dye.

Dye discloses a memory controller that includes embedded data compression and decompression engines and uses data compression to reduce system bottlenecks. However, the system structure that is disclosed by Dye is distinct from that of the system that is set forth in the Applicant's claims and cannot support significant aspects of the functionality of the system that

is defined in Applicant's claims. Specifically, Dye does not show a controller graphics engine that includes an integral interface where the data that is transmittable to a coupled FIFO buffer is transmitted via the integral interface as is set forth in Claim 1 (independent Claims 11 and 20 contain similar limitations).

In the Office Action, instruction storage/decode 230 shown in Dye, is equated with the recited FIFO buffer. Applicant respectfully submits that a FIFO buffer is a notoriously well known type of storage component and would not reasonably be confused with instruction storage/decode logic 230 by one of ordinary skill in the art. Accordingly, there is no structure disclosed by Dye that can be reasonably equated to the recited FIFO buffer that is controlled via an interface that is integral with a graphics engine. It should be appreciated that the portions of the Dye (col. 12 line 17 and col. 3 lines 10-13) reference that are referenced in the instant rejection do not in any way confuse the disclosed storage/decode logic 230 with a FIFO buffer. Accordingly, the strained characterizations of the Dye system made in the outstanding Office Action that includes characterizing storage/decode logic 230 as being a FIFO buffer are not supported by the subject matter that is disclosed in Dye.

For the reasons outlined above, Applicant respectfully submits that Claims 1, 11 and 20 are in condition for allowance. Furthermore, Applicant respectfully submits that Dye does not anticipate or render obvious the embodiments of the present claimed invention as are set forth in Claims 9-10 dependent on Claim 1 and Claim 16 dependent on Claim 11. Accordingly, Claims 9-10 and 16 are likewise allowable as they are dependent on allowable base Claims 1 and 11.

103 Rejection

Claims 3-8, 13-15, 17-20 and 22-28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dye (U.S. Patent No. 6,173,381) in view of Davis et al. (U.S. Patent No.

4,991,169). The Applicant has reviewed the cited references and respectfully submits that embodiments of the present invention as are set forth in Claims 3-8, 13-15, 17-20 and 22-28 are neither anticipated nor rendered obvious by Dye in view of Davis et al.

The Examiner is respectfully directed to independent Claim 1 from which rejected Claims 3-8 depend and which recites limitations similar to those recited in independent Claims 11 and 20 from which rejected Claims 13-15 and 17-19 and rejected Claims 22-28 respectively depend. Claim 1 is presented below in its entirety for the Examiner's convenient reference.

> 1. A controller chip comprising:
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> a graphics engine operative to manage a memory, the graphics engine comprising an integral interface; and
>
> a first in first out (FIFO) buffer coupled to the graphics engine, the FIFO buffer being accessible by a central processing unit (CPU) through the graphics engine, wherein the graphics engine receives commands from the CPU via the integral interface, and manages the FIFO buffer via the integral interface wherein data transmittable to the FIFO buffer is transmitted via the integral interface.

Dye in view of Davis et al. does not anticipate or render obvious the embodiments of the present claimed invention as set forth in Claims 3-8, 13-15, 17-20 and 22-28. Dye in view of Davis et al. is deficient as Dye in view of Davis et al. does not teach or suggest each of the limitations of these Claims as is required to anticipate or render them obvious. In particular, Dye does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer where "data transmittable to the FIFO buffer is transmitted via the integral interface" as is recited in Claim 1 (from which, as alluded to above, rejected Claims 3-8 depend and which recites limitations similar to those recited in independent Claims

11 and 20 from which rejected Claims 13-15 and 17-19 and rejected Claims 22-28 respectively depend). And, Davis does not teach these limitations to remedy the deficiencies of Dye.

Davis et al. only shows a dual digital signal processor that provides real time links between multiple time division channels of a digital carrier signal. It should be appreciated that Davis et al. is concerned with providing a system that has the capacity to mediate communications between a carrier and a host system. However, nowhere in the Davis et al. reference is there shown a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer where "data transmittable to the FIFO buffer is transmitted via the integral interface" as is recited in Claim 1 (from which rejected Claims 3-8 depend, and which recites limitations similar to those recited in independent Claims 11 and 20 from which rejected Claims 13-15 and 17-19 and rejected Claims 22-28 respectively depend).

In addition, Applicant respectfully submits that Dye in view of Davis does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer that includes the above discussed limitations of Claim 1 (from which Claim 3 depends) and further includes the limitation "in which the FIFO buffer comprises a circular FIFO buffer" as is set forth in dependent Claim 3. Moreover, Applicant respectfully submits that Dye in view of Davis does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer that includes limitations of Claim 1 discussed above and that further includes the limitation "in which the FIFO buffer comprises a double buffer" as is set forth in dependent Claim 4.

In addition, Applicant respectfully submits that Dye in view of Davis et al. does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer that includes the above discussed limitations of Claim 1 and

further includes the limitation "in which the FIFO buffer comprises a triple buffer" as is set forth in dependent Claim 5. Moreover, Applicant respectfully submits that Dye in view of Davis et al. does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer that includes the above discussed limitations of Claim 1 and further includes the limitation "wherein the effective size of the FIFO buffer as viewed by the CPU can be as large as the memory" as is set forth in dependent Claim 6.

In addition, Applicant respectfully submits that Dye in view of Davis et al. does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer that includes the above discussed limitations of Claim 1 and further includes "a checking mechanism for determining if the FIFO buffer needs to be emptied without utilizing the CPU" as is set forth in dependent Claim 7. Moreover, Applicant respectfully submits that Dye in view of Davis et al. does not teach or suggest a controller chip comprising a graphics engine (that comprises an integral interface) and a first in first out (FIFO) buffer that includes the above discussed limitations of Claim 1 and further includes a checking mechanism that comprises: means for calculating the time required to fill the FIFO buffer; means for determining if the used memory of the FIFO buffer, is below a predetermined amount based upon the time required to fill the FIFO buffer; and means for preventing the FIFO buffer from filling if the used memory in the FIFO buffer is over the predetermined amount as is set forth in dependent Claim 8. Claims 13-15 and 17-19 dependent on Claim 11 and Claims 22-28 dependent on Claim 20 recite limitations similar to those recited in Claims 3-8 and are allowable for similar reasons.

For the reasons outlined above, Applicant respectfully submits that Dye in view of Davis et al. does not anticipate or render obvious the embodiments of the present claimed invention as are recited in Claims 3-8 dependent on Claim 1, Claims 13-15 and 17-19 dependent on Claim 11 and Claims 22-28 dependent on Claim 20. Accordingly, Claims 3-8, 13-15 and 17-19 and 22-28

are allowable as they are dependent on allowable base Claims and as they recite additional limitations not taught or suggested by Dye in view of Davis.

Conclusion

In light of the above-listed remarks, the Applicant respectfully requests allowance of the remaining Claims.

The Examiner is urged to contact the Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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